A 7.9-9.7GHz On-Chip Radar Receiver Front-End For Future Adaptive X-Band Smart Skin Array Antennas

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Abstract — **In this paper, we present a 7.9-9.7GHz on-chip radar receiver front-end intended for a digital beamforming X-band smart skin phased array antenna. This agile single-chip receiver front-end could potentially enable a significant size and cost reduction of the microwave receiver modules in such an adaptive frequency hopping radar system. Measured results show a close to adequate performance.**

I. Introduction

To minimize the vulnerability to jamming signals is essential in modern radar systems. In a frequency hopping radar the transmitter and the receiver jump in a random like way between different selected frequencies. To further reduce the vulnerability to electromagnetic interference (EMI) and jamming adaptive methods and digital beamforming can be employed [1].

Many airborne radar systems are typically designed to operate at X-band (8-12GHz) or above (partly due to obvious restrictions on the maximum allowable dimensions of the radar hardware). Frequency hopping adaptive X-band radar systems may in the future rely on compact conformal phased array antennas that can be confined inside the metallic surface of a vessel or an aircraft, for example, so called "smart skin" antennas [2]. In such multi-channel adaptive radar array antennas the number of microwave receiver modules required can be as high as several hundreds. To minimize size and cost of each receiver module is therefore becoming increasingly important. Despite this demand, microwave receivers are traditionally being fabricated using hybrid circuit technologies that are neither compact nor very suitable for low-cost production [1]. Thus, to be able to realize multi-channel radar systems that are much more compact and cost-effective, low-cost integration methods that can be used to reduce the microwave receiver size and complexity have to be developed. As a consequence of this, increased interest has recently been focused on the possibilities of using frequency tunable high gain and low noise active monolithic microwave integrated circuit (MMIC) filters to reduce the vulnerable bandwidth of future adaptive frequency hopping radar systems [3]. If such a bandpass filter is integrated on the same die as an MMIC image rejection mixer, a single-chip receiver front-end that combines the attractive feature of small size at low cost with good ability to reject out-of-band signals could potentially be realized. Such a front-end could possibly also reduce the number of down-converting stages required in an agile radar receiver by allowing a greater down-conversion step to be made. Rejection at the receiver image frequency should however be high enough to avoid the effect of any interfering signals that may be present at this frequency. In other words, the total image rejection of the receiver (front-end) should be in the same order as the required spurious-free dynamic range (SFDR) [1]. A schematic description of a single-chip front-end of the type described above is shown in Fig. 1.

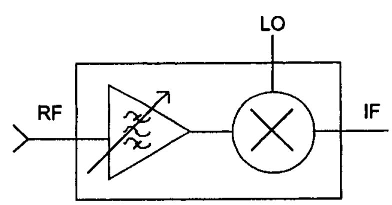

Fig. 1. Block diagram of a single-chip receiver front-end composed of a frequency tunable high gain and low noise active MMIC filter and an image rejection MMIC mixer.

Typical requirements for the receiver front-ends of future adaptive X-band radar antennas are summarized in Table I. The specification is based on our experience in the area and on assumed radar system requirements. Note that an SFDR of 109dB/Hz$^{2/3}$ corresponds to an SFDR of 60dB when a noise bandwidth (B) of 20MHz is assumed.

TABLE I
TYPICAL RECEIVER FRONT-END REQUIREMENTS IN FUTURE ADAPTIVE X-BAND RADAR ANTENNAS.

Relative agile bandwidth	20-40%
Noise figure (NF)	<5 dB
Input third order intercept point (IIP_3)	≥-6 dBm
Spurious-free dynamic range (SFDR)	≥109dB/Hz$^{2/3}$

To our knowledge, relatively few papers have been published on the realization of fully monolithically integrated agile image reject receiver front-ends at X-band or above. Zelley [4] presented a 12-18GHz single-chip radar transceiver with 20dB of image rejection. An 8.7-9.8GHz two-chip filter/mixer front-end was presented in [3]. In this paper, we present of a 7.9-9.7GHz single-chip radar receiver front-end intended for the microwave receiver modules of an adaptive smart skin array antenna. This front-end is based on two previously developed X-band circuits: a tunable active MMIC filter [5] and an image rejection MMIC mixer [6]. The design of these two MMIC's and the combined single-chip front-end are shortly described in section II. Finally, in Section III experimental results of the front-end are compared with the corresponding measured data obtained from break out circuits that contain the filter and the mixer used in the front-end.

II. On-Chip X-Band Radar Receiver Front-End

A. Tunable Active Low Noise Filter

Recursive active MMIC filters are promising for narrow band and low noise applications since high-Q filters of this type can be designed with high gain in combination with a noise figure approaching that of the low noise amplifier (LNA) used in the filters [7]. Such filters could thus potentially replace the traditional cascade of an LNA and a passive filter (that often are rather bulky). Promising filter solutions when we consider tunable active X-band MMIC filters with a relative tuning range in the order of 15-20% are, for example, presented in [3] and [8]. These two designs suffer however from either a too low out-of-band rejection or a noise and large signal performance that is inadequate for our application in mind. A frequency tunable X-band active MMIC bandpass filter which according to simulations could achieve a sufficiently high filter out-of-band rejection while also being able to fulfil typical X-band radar receiver noise and large signal requirements is on the other hand presented in [5]. The chosen filter implementation consists of two identical (second order) recursive active filters placed between two quadrature couplers. The filter center frequency tuning is implemented using the novel concept of self-switched (three-bit) time shifters that enable (eight) discrete filter tuning states [8].

B. Image Rejection Mixer

In our proposed on-chip front-end solution a mixer with a relatively high internal image rejection is typically needed. The mixer should also have high isolation between the RF and LO ports. To meet these demands a classic double balanced mixer where the mixing stages are implemented using dual-gate field effect transistors (FET's) could be used. To achieve high values of image rejection implies however tough requirements on phase and amplitude balance of such a mixer, something that can be rather difficult to maintain over a large bandwidth. Therefore this type of mixer normally has two ways of operating, fixed or tuned DC bias for the dual-gate FET based mixing stages. With fixed bias we mean that the mixer DC biasing conditions are kept constant for all frequencies. Tuned bias means on the other hand that the DC voltages applied to the dual-gate FET mixing stages are varied in order to obtain the best possible phase and amplitude balance at each frequency of interest. To obtain the highest possible image rejection over a large bandwidth for a double balanced mixer implies therefore that we allow the mixer DC biasing to be tuned. The MMIC image rejection mixer used in our proposed single-chip front-end is based on a double balanced 1GHz-IF mixer design presented in [6]. According to measurement results of this mixer, an image rejection of 45-50dB can be obtained over the X-band when the mixer bias is tuned. The corresponding result in the case of fixed bias is 18-20dB. The RF to IF conversion loss is typically 10dB.

C. Single-Chip Front-End

With reference to the filter and mixer designs described above, we have designed an on-chip 1GHz-IF X-band front-end by cascading these two circuits on the same die. Figure 2 shows a photo of the single-chip X-band receiver front-end. In this design all circuitry needed for impedance matching and transistor biasing is included on-chip. However, in order to be able to experimentally evaluate the front-end it had to be mounted in a test fixture. All RF and DC bias pads were therefore connected using bonding-wires. The front-end was fabricated using a 0.2µm GaAs/AlGaAs PHEMT based MMIC process.

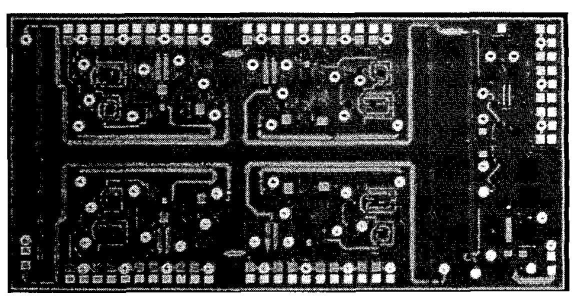

Fig. 2. Photo of the single-chip X-band receiver front-end composed of a tunable active filter (to the left) and an image rejection mixer (to the right). Chip dimensions: 3mmx6mm.

TABLE II

SUMMARY OF RESULTS

Measured Results	Max Image rejection [dB]	Gain [dB]	NF [dB]	P_{1dB}(input) [dBm]	IIP_3 [dBm]	SFDR* [dB] *B=20MHz
Front-end	60	0	≥7^(†)	-5 to –2	≈0	≤63
Filter [5]	20-23	11-16	6	Not Available	≈0	≈63
Mixer	47-50	-10 to –8	11-13	0-2	6-8	64

(†) *Estimated result based on the measured filter and mixer data.*

V. RESULTS

Figure 3 and 4 show measured image rejection and conversion gain for the front-end in the case of fixed and tuned mixer bias respectively. The measured results have been obtained at all eight possible tuning states of the filter corresponding to filter center frequencies ranging from 7.9-9.7GHz (i.e. over a relative agile bandwidth of 20%). With fixed mixer bias we mean that the mixer bias is kept constant at all filter tuning states. Tuned mixer bias means on the other hand that the mixer bias is separately tuned to obtain maximum possible image rejection at each filter tuning state. In both cases the RF input power was 0dBm and the LO power was 10dBm.

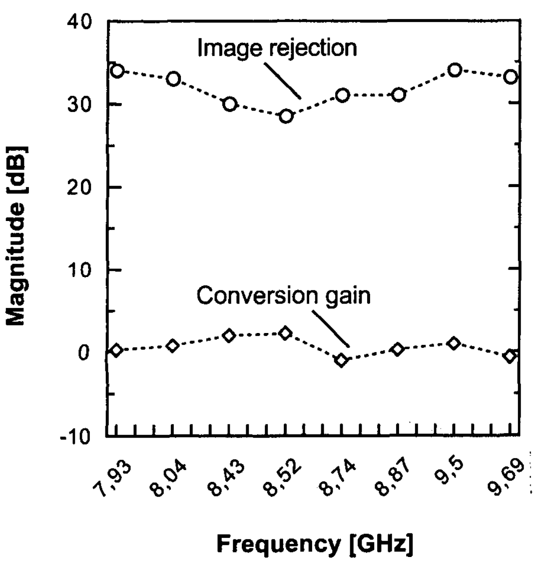

Fig. 3. Measured image rejection and conversion gain for the front-end in the case of fixed mixer bias at each filter center frequency tuning state (P_{DC}=840mW).

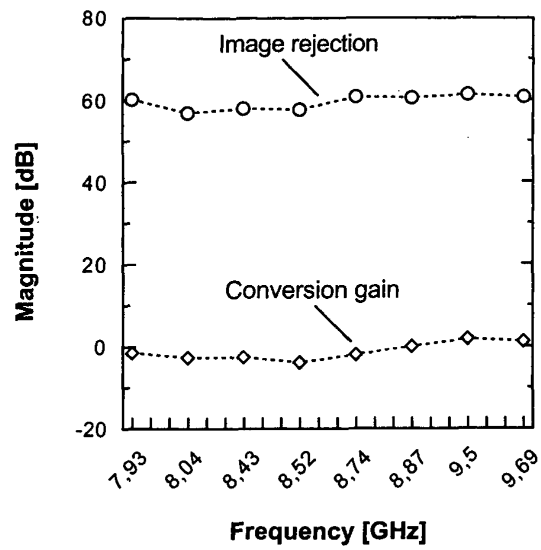

Fig. 4. Measured image rejection and conversion gain for the front-end when the mixer bias is tuned to obtain maximum possible mixer image rejection at each filter center frequency tuning state (P_{DC}=840mW).

As can be seen from Fig. 3 the maximum image rejection that can be achieved for the front-end at an IF of 1GHz in the case of fixed mixer bias varies between 30-35dB over the agile frequency band. The corresponding result with tuned mixer bias is 60dB (see Fig. 4). The front-end conversion gain is in both cases around 0dB. The filter and mixer DC currents are 230mA and 30mA from 3V and 5V DC supply, respectively. These values correspond to 840mW of DC power dissipation (P_{DC}).

Typical measured front-end data over the agile frequency band are summarized in Table II. Measured filter data obtained from a break out circuit that contain the filter used in the front-end are presented in [5]. These data are together with the corresponding measured data of the mixer also shown in Table II. We may note from Table II that the typically measured maximum value of front-end image rejection is about 10dB lower than the sum of the measured maximum values of filter and mixer image rejection respectively. A similar deviation can also be found at the higher tuning states between the typical measured value of front-end conversion gain and the sum of the corresponding measured values of filter and mixer conversion gain respectively. It should however be noted that the measured mixer data are obtained at different bias conditions (40mA from 2V DC supply) than those used during measurement of the front-end (30mA from 5V DC supply). Furthermore, the rather limited dynamic range of the measurement equipment used resulted in that a relatively high RF input power of 0dBm was required in order to be able to measure the maximum possible front-end image rejection. At such a high value of input power the filter and thereby also the front-end are in their saturated region of operation. This implies that the front-end possibly could have a maximum image rejection and conversion gain that are somewhat higher than the values we obtained during measurement. Another possible explanation to the discrepancy between measured and expected values of front-end image rejection and conversion gain respectively could be filter and mixer impedance mismatching.

At this point, we have not been able to measure the noise figure of the front-end. However, based on measured filter and mixer data the noise figure of the combined filter/mixer front-end is estimated at 7dB. Table II shows that the input-referred 1dB compression point (P_{1dB}) of the front-end varies between –5 to –2dBm over the agile bandwidth. The corresponding typical measured value of front-end IIP_3 is approximately 0dBm. If we combine this result with the estimated value of front-end NF we obtain more than 60dB of front-end SFDR when a noise bandwidth of 20MHz is assumed. A comparison of the experimentally obtained results with the typical requirements given in Table I indicates that the performance of the evaluated front-end is close to adequate for the microwave receiver modules of a digital beamforming X-band smart skin radar antenna, for example. Compared with more conventional microwave front-ends (that are fabricated using hybrid circuit components) the proposed front-end could potentially enable a significant reduction of the microwave receiver size and complexity in such a future adaptive radar system.

VI. Conclusion

A 7.9-9.7GHz single-chip receiver front-end composed of a tunable active MMIC filter and an image rejection MMIC mixer has been presented. Measurement results show that this front-end can achieve an image rejection of 60dB which is in the same order as the typically required spurious-free dynamic range. Estimations based on measured data of the filter and of the mixer imply that the evaluated front-end can also achieve a noise and large signal performance that is close to what should be adequate for the microwave receivers of future adaptive X-band radar systems. The use of such an agile on-chip front-end is expected to result in a significant reduction of size and cost of the microwave receiver modules in digital beamforming X-band smart skin radar array antennas, for example.

Acknowledgement

This work was financially supported by *The Swedish Armed Forces (FM)*.

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